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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,842	07/31/2003	Chia-Ta Hsieh	252016-2390	1038

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/631,842	HSIEH, CHIA-TA	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 08/08/2005, claims 16-63 are active in this application.

New claims 60-63 have been added.

Correction(s) to the drawing filed 08/08/2005 have been considered and accepted.

Remarks

2. Applicant's argument(s) filed 08/08/2005 has/have been fully considered, but are moot in view of the new ground of rejection(s).

Claim Rejections - 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim(s) 16-24, 26-36, 38-46, 48-57, and 59-63 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,278,438 to Kim et al.

Regarding claims 16, and 28, Kim discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-13, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 13 over said semiconductor region (figs. 1-6);

forming, sequentially, a conductive layer 14/16, an insulator layer 15/19 and a hard mask layer 17 over said gate insulator layer 15;

patterning said gate insulator layer 13, said conductive layer 14/16, said insulator layer 15/19 and said hard mask layer 17 to form a plurality of tiered parallel stripes;

forming a spacer insulator layer 26/28 over the sidewalls of said parallel stripes;

forming trenches 30/42 in said semiconductor region between said parallel stripes;

growing an insulator liner layer (trench surface protection oxidation layer, fig. 5-6 and col. 5, lines 28-66; col. 6, lines 30-31) over sides of said trenches 30/42 and underlying said spacer insulator 26/28, and depositing an insulator filler layer (LTO) so that said trenches 30/42 and the space 26/28 between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated conductive regions, or separate floating gates (col. 5, lines 28-46, and figs. 1-6, 13).

Regarding claims 39, and 50 Kim discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-13, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 13 over said semiconductor region;

forming, sequentially, a conductive layer 14/16 and an insulator layer 15/19 over said gate insulator layer 13;

patterning said gate insulator layer 13, said conductive layer 14/16 and said insulator layer 15/19 to form a plurality of tiered parallel stripes;

forming a spacer insulator layer 26/28 over the sidewalls of said parallel stripes;

forming trenches 30/42 in said semiconductor region between said parallel stripes;

growing an insulator liner layer (trench surface protection oxidation layer, figs. 5-6, and col. 5, lines 28-66; col. 6, lines 30-31) over sides of said trenches 30/42 and underlying said spacer insulator 26/28 and depositing an insulator filler layer (LTO) so that said trenches 30/42 and the space between said parallel stripes are filled with said insulator tiller layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer;

patterning said conductive layer to form separated conductive regions, or separated floating gates (col. 5, lines 28-46, and figs. 1-6, 13).

Regarding claims 17, 29, 40, and 51, Kim discloses the method wherein said semiconductor region is a silicon region. See col. 5, lines 1-14.

Regarding claims 18, 30, 41, and 52, Kim discloses the method wherein said substrate is a silicon substrate. See col. 5, lines 1-14.

Regarding claims 19, 31, 42, and 53, Kim discloses the method wherein said gate insulator regions are oxide regions. See col. 3, lines 52-53.

Regarding claims 20, 32, 43, and 54, Kim discloses the method wherein said insulator liner layer is a grown oxide layer. See figs. 5-6, and col. 5, lines 28-66; col. 6, lines 30-31.

Regarding claims 21, 33, 44, and 55, Kim discloses the method wherein said insulator filler layer is an HDP oxide layer. See col. 3, line 35 to col. 6, line 62.

Regarding claims 22, 34, 45, and 56, Kim discloses the method wherein said conductive layer is composed of doped polysilicon. Col. 3, lines 45-66.

Regarding claims 23, 35, 46, and 57, Kim discloses the method wherein said insulator layer 19 is a nitride layer. See col. 3, lines 45-66.

Regarding claims 24, and 36, Kim discloses the method wherein said hard mask layer 17 is an oxide layer. See col. 3, lines 45-66.

Regarding claims 26, 38, 48, and 59, Kim discloses the method comprising all claimed limitations. See col. 3, line 35 to col. 6, line 62.

Regarding claims 27, and 49, Kim discloses the method wherein said conductive regions are gates of semiconductor integrated circuit devices. See figs. 1-6.

Regarding claims 60-63, Kim discloses the method wherein the spacer insulator layer 26/28 is on the insulator liner layer. See figs. 5-6.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim(s) 25, 37, 47, and 58 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,278,438 to Kim et al., in view of the following remarks.

Regarding claims 25, 37, 47, and 58, Kim discloses the method wherein said insulator spacer layer is an oxide layer, instead of a nitride layer.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kim so that the spacer layers being form of nitride, which is well known in the art, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claim(s) 16, 28, 39, and 50 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,851,881 to Lin et al., in view of Mendicino, U.S. Patent No. 6,271,143.

Regarding claims 16 and 28, Lin discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-3, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 30 (or 41 (over the MONOS gate area 24 and source/trench area 79)) over said semiconductor region 10;

forming, sequentially, a conductive layer 32 (or 44), an insulator layer 41 (or 42)

and a hard mask layer 42 (or 43) over said gate insulator layer 30;

patterning said gate insulator layer 30 (or 41), said conductive layer 32 (or 44), said insulator layer 41 (or 42) and said hard mask layer 42 (or 43) to form a plurality of tiered parallel stripes;

forming a spacer insulator layer 47 over the sidewalls of said parallel stripes;

forming trenches 71 in said semiconductor region 10 between said parallel stripes; wherein the trenches are underlying the spacer insulator;

depositing an insulator filler layer 70 so that said trenches 71 and the space between said parallel stripes are filled with said insulator filler layer 70;

planarizing so that said insulator filler layer 70 above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches (see col. 6, lines 37-41);

removing said insulator layer 30/41 and said insulator spacer layer 47;

patterning said conductive layer to form separated conductive regions, or separated floating gate.

See also col. 4, line 47 to col. 6, line 57.

Lin does not explicitly discuss about growing an insulator liner layer over sides of the trenches and underlying said spacer insulator.

Mendicino discloses a method for creating a trench isolation, as shown in figs. 1-13, comprising isolation trenches, a liner layer formed over the sidewalls of the trenches, and isolation layer/filler formed on the liner layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lin so that it would further include a liner layer over the sidewalls of the trenches, as that of Mendicino, in order to reduce or prevent the trench fill erosion, thereby eliminating or reducing the adverse device affects of the parasitic sidewall. See col. 1, line 21 to col. 3, line 49; and col. 4, lines 10-14 of Mendicino. Note that since the isolation trenches are underlying the spacer insulator, and the liner layer is formed over the sidewalls of the trench and within the trench; therefore the liner layer must also be underlying the spacer insulator.

Regarding claims 39 and 50, Lin discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-3, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 30 (or 41, (over the MONOS gate area 24 and source/trench area 79)) over said semiconductor region 10;

forming, sequentially, a conductive layer 32 (or 44) and an insulator layer 41 (or 42 over said gate insulator layer;

patterning said gate insulator layer 30/41, said conductive layer 32/44 and said insulator layer 30/41 to form a plurality of tiered parallel stripes;

forming a spacer insulator layer 47 over the sidewalls of said parallel stripes;

forming trenches 71 in said semiconductor region 10 between said parallel stripes; wherein the trenches are underlying the spacer insulator;

depositing an insulator filler layer 70 so that said trenches and the space between said parallel stripes are filled with said insulator filler layer 70;

planarizing so that said insulator filler layer 70 above top of said insulator layer is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer 41/42 and said insulator spacer layer 47;

patterning said conductive layer 32/44 to form separated conductive regions, or to form separated floating gates. See also col. 4, line 47 to col. 6, line 57.

Lin does not explicitly discuss about growing an insulator liner layer over sides of the trenches and underlying said spacer insulator.

Mendicino discloses a method for creating a trench isolation, as shown in figs. 1-13, comprising isolation trenches, a liner layer formed over the sidewalls of the trenches, and isolation layer/filler formed on the liner layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Lin so that it would further include a liner layer over the sidewalls of the trenches, as that of Mendicino, in order to reduce or prevent the trench fill erosion, thereby eliminating or reducing the adverse device affects of the parasitic sidewall. See col. 1, line 21 to col. 3, line 49; and col. 4, lines 10-14 of

Mendicino. Note that since the isolation trenches are underlying the spacer insulator, and the liner layer is formed over the sidewalls of the trench and within the trench; therefore the liner layer must also be underlying the spacer insulator.

Conclusion

8. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
October 21, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Replacement Sheet

Accepted
dhn
10/21/2005

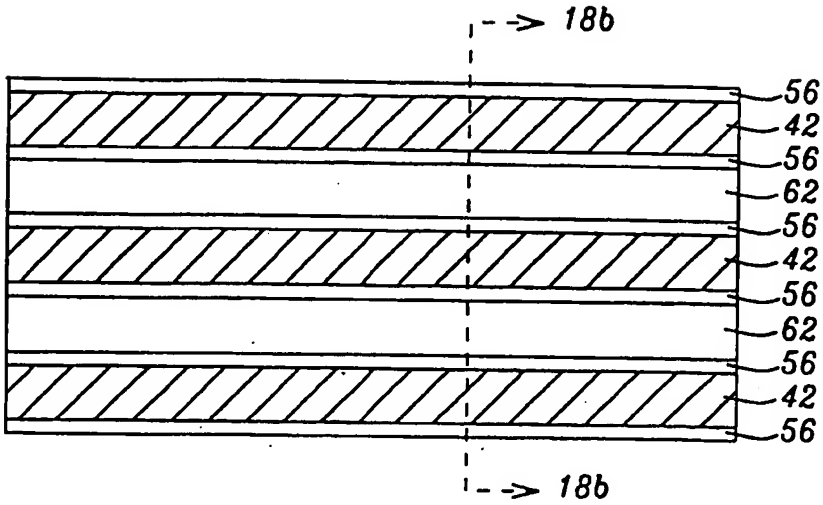

FIG. 18a

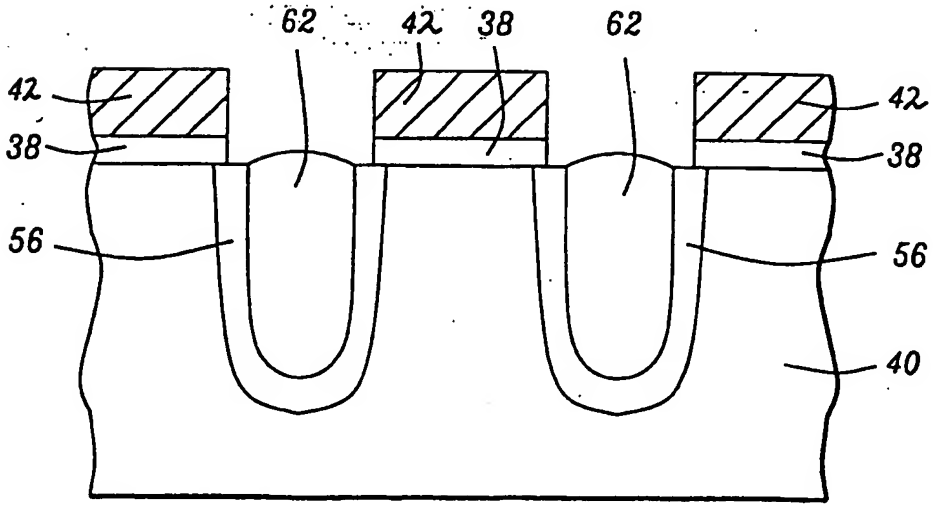

FIG. 18b